Nanoimprint System Development and Status for High Volume Semiconductor Manufacturing

Tsuneo Takashima[1], Yukio Takabayashi[1], Naosuke Nishimura[1], Keiji Emoto[1], Takahiro Matsumoto[1], Tatsuya Hayashi[1], Atsushi Kimura[1], Jin Choi[2], Phil Schumaker[2],
[1]Canon Inc., 20-2, Kiyohara-Kogyodanchi, Utsunomiya-shi, Tochigi 321-3292 Japan
[2]Canon Nanotechnologies, Inc., 18707 West Braker Lane, Austin, TX USA

Abstract

Imprint lithography has been shown to be an effective technique for replication of nano-scale features. Jet and Flash* Imprint Lithography (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

Criteria specific to any lithographic process for the semiconductor industry include overlay, throughput and defectivity. The purpose of this paper is to describe the technology advancements made overlay, throughput and defectivity and to introduce the FPA-1200NZ2C cluster system designed for high volume manufacturing of semiconductor devices. in the reduction of particle adders in an imprint tool and introduce the new mask replication tool that will enable the fabrication of replica masks with added residual image placement errors suitable for memory devices with half pitches smaller than 15nm.

Overlay results better than 5nm 3sigma have been demonstrated. To further enhance overlay, wafer chucks with improved flatness have been implemented to reduce distortion at the wafer edge. To address higher order corrections, a two part solution is discussed. An array of piezo actuators can be applied to enable linear corrections. Additional reductions in distortion can then be addressed by the local heating of a wafer field.

The NZ2C cluster platform for high volume manufacturing is also discussed. System development continues this year with a target for introduction later in 2016. The first application is likely to be NAND Flash memory, and eventual use for DRAM and logic devices as both overlay and defectivity improve.

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

Keywords: Jet and Flash Imprint Lithography, J-FIL, nanoimprint lithography, NIL, overlay, throughput, defectivity, particles, mask life

1. Introduction

The path towards denser devices with reduced critical dimensions and greater functionality is the cornerstone of the semiconductor industry. Immersion lithography, along with the development of multiple patterning techniques has allowed device manufacturers to realize half pitch designs as small as 15nm. Self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP) processes were instrumental in accelerating the fabrication of new generations of NAND Flash memory, and the same patterning techniques are now being adopted for use in DRAM and logic devices.[1,2]

The drawbacks to these patterning approaches mainly center on yield and cost. Many extra deposition, etch and lithography steps are required which impact device cost and performance. Lithographic technologies that can directly image finer features without the need for additional processing are very appealing, as long as they can produce yields comparable to state of the art devices.

Imprint lithography is an effective technique for replication of nano-scale features.[3,4] Jet and Flash Imprint Lithography (J-FIL) involves the field-by-field deposition and exposure of a low viscosity resist deposited by Drop-On-Demand inkjet onto the substrate.[5-10] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Alternative Lithographic Technologies VIII, edited by Christopher Bencher, Proc. of SPIE Vol. 9777, 977706 · © 2015 SPIE · CCC code: 0277-786X/15/$18 · doi: 10.1117/12.2219001

Previous studies have demonstrated J-FIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Figure 1 compares relative cost per wafer level for three different lithographic approaches, including imprint lithography. When compared to an immersion based Self Aligned Quadruple Patterning (SAQP), approach, Cost of Ownership (CoO) for Nanoimprint Lithography (NIL) is reduced by approximately 40%.

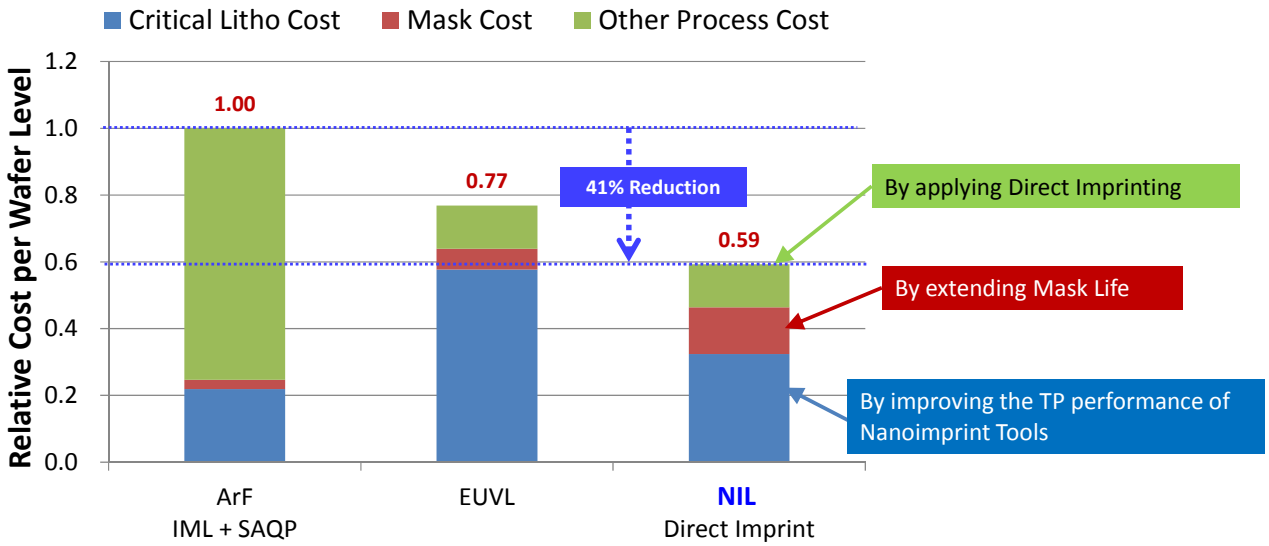


Figure 1. Cost of Ownership comparison for different lithographic processes.

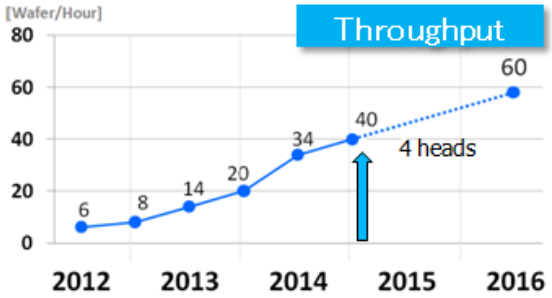
There are many criteria in addition to resolution that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both CDU and line edge roughness meet the criteria of 2nm. A collaboration partner has achieved overlay of 10nm (with a target of 8nm)[11] and defect levels ~ 5/cm^2 across a lot of 25 wafers.[12] Other criteria specific to any lithographic process include throughput, which plays a strong role in determining whether Cost of Ownership requirements can be met. Recently, Takeishi and Sreenivasan reported that a throughput of 40 wafers per hour was achieved on a four station imprint tool.[13]

On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photomasks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6" x 6" x 0.25" fused silica was reported to have a defectivity of only 0.04/cm^2 as measured by a Lasertec tool with 50 nm sensitivity.[14] Recently, Ichimura et al. have exceeded the targets for both CDU and IP. In addition, master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20 nm have been fabricated.[15]

The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. In 2012, an MR-5000 mask replication tool was developed specifically to pattern replica masks from an e-beam written master. Previous work by Ichimura et al. using this tool, demonstrated that a CDU of less than 1.5nm 3σ can be achieved on both the master and replica masks.[16] In 2012, an MR-5000 mask replication tool was developed specifically to pattern 6" x 6" x 0.25" replica masks from an e-beam written master.

In 2015, Canon Inc. introduced the FPA-1100NZ2. The NZ2 has a footprint smaller than an i-line tool, and has throughput and overlay specifications of 10 wafers per hour and 8nm, respectively.[13] The system is suitable for pilot

scale operation, device fabrication demonstration and process module development. Representative data collected from the NZ2 is shown in Figure 2. Throughput was described for a four system approach and was 40 wafers per hour. A defect density of 9 defects/cm^2 was reported and champion overlay less than 5nm 3sigma was achieved.



Mix and Match Overlay

	X	Y
Average	-0.3 nm	0.1 nm
3σ	3.9 nm	4.7 nm
|Ave.|+3σ	4.2 nm	4.8 nm

Figure 2. Data from the NZ2 system

The purpose of this paper is to describe the technical progress over the last year and to introduce the NZ2C four station platform designed for high volume manufacturing.

2. Technical Progress

Figure 3 presents an overview of progress made over the last several years and also describes direction for the future. The four graphs in the figure document the key indicators of imprint technology, which include overlay, throughput, defectivity and particle reduction on the wafer. Presently, throughput of 60 wafers per hour has been demonstrated, with champion overlay results of less than 5nm, defectivity of 5 defects/cm^2, and particles per wafer pass of 0.003. Details on these four indicators are described in the next four sections.

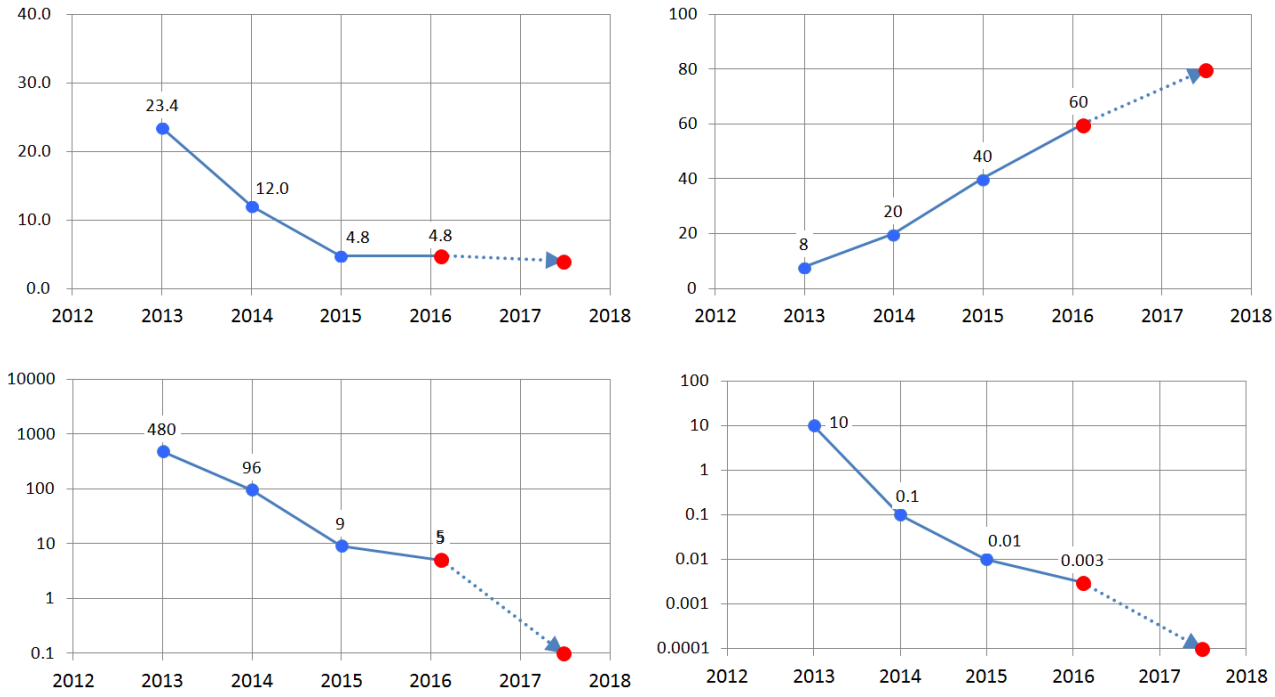


Figure 3. History, status on roadmaps for overlay, throughput, defectivity and particles.

a. Overlay

Using a through the mask (TTM) alignment system, 1nm repeatability has been demonstrated. To realize improved overlay results, it will be necessary to address wafer chuck flatness issues that introduce distortion, particularly towards the edge of the wafer. Figure 4 shows the advantages of an improved wafer chuck. The figures across the top describe a wafer chuck that induced an image placement error of approximately 9nm at the wafer edge. By reducing chuck flatness, local deformations were reduced to about 4nm.

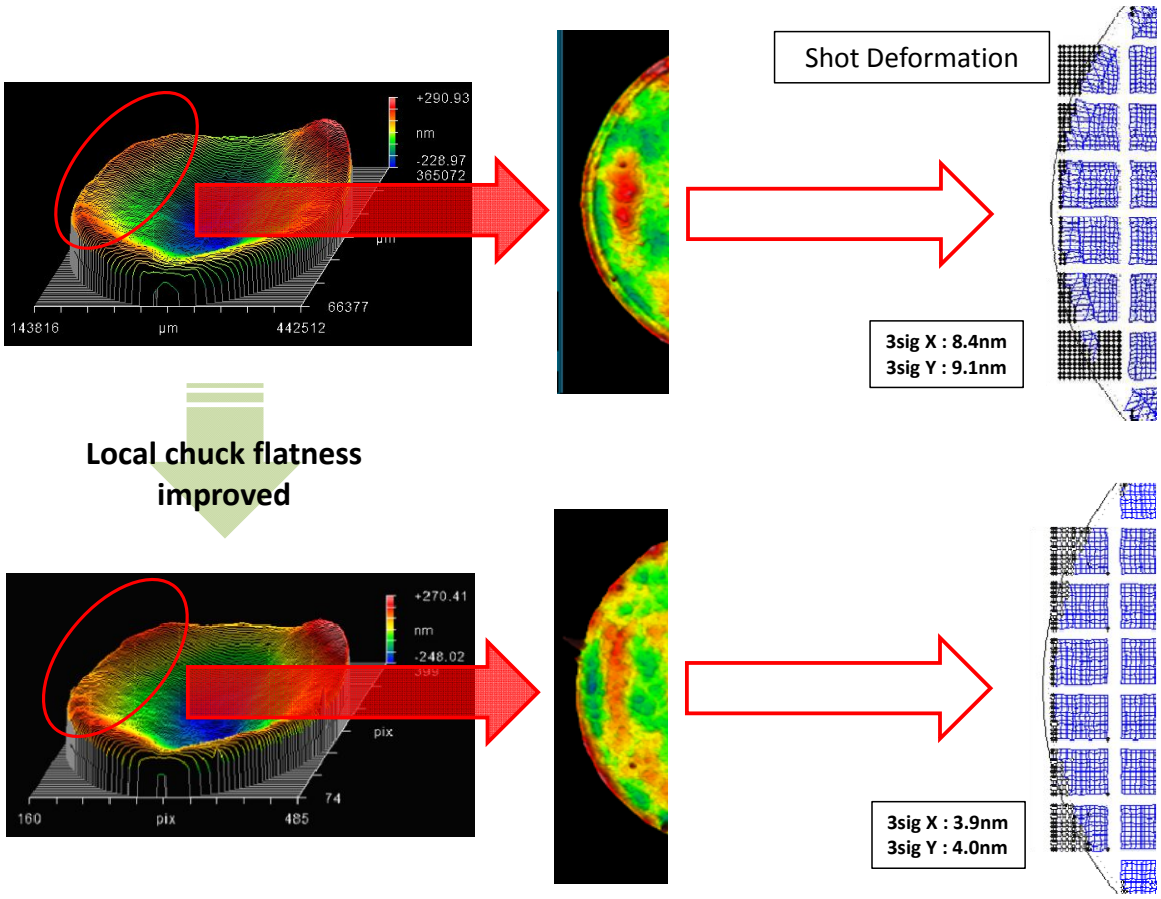


Figure 4. The effect of wafer chuck flatness on shot deformation for two different wafer chuck configurations.

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, Shot Shape High Order Compensation (SSHOC) is done by manipulating both the stage and lens during the exposure process. A different approach is required for the imprint tool in order to do high order corrections (HOC). HOC for NIL can be enabled by combining two approaches:

1. Mag actuator, which applies force using an array of piezo actuators
2. Heat input to correct distortion on a field by field basis

Both approaches are described below.

With respect to the mag actuator, a larger array of piezo based actuators can be applied to do linear corrections. A simple schematic is shown in Figure 5.

Heat input on a field by field basis is also possible, and defines a potential path for achieving overlay results of better than 3nm. An example of this method is depicted in Figure 6. Figure 6a describes the heat input, temperature and initial shot distortion at time T = 0. Figure 6b shows the final heat input, temperature and distortion after 500 msec, which is well within the resist fill time budget of 1000 msec to achieve throughputs of 20 wafers per hour per imprint station.

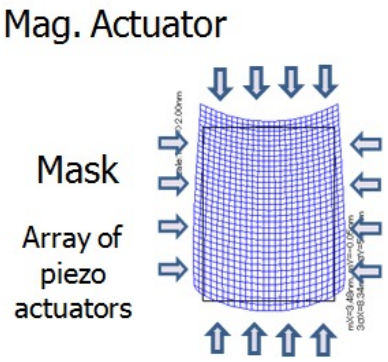


Figure 5. HOC correction using an array of piezo actuators.

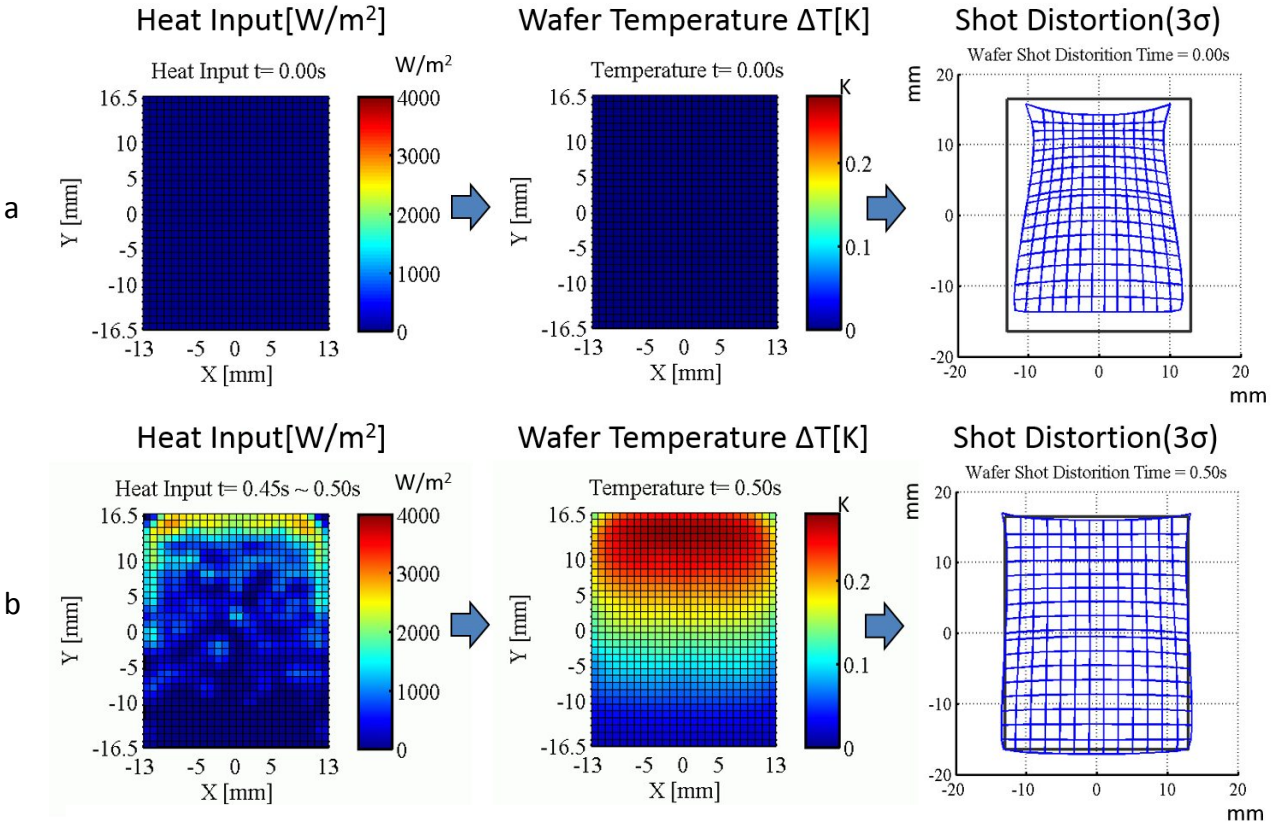


Figure 6. a) Shot distortion at time T = 0. B) Distortion after a heat input of 500 msec.

Initial heat input experiments have now been performed and the results are very promising. Simulation and experimental results are in excellent agreement, and a reproducibility across a four wafer set of ~1nm was demonstrated. Further studies will be reported at a later date.

b. Throughput

There are several parameters that can impact resist filling. Key parameters include resist drop volume (smaller is better), system controls (which address drop spreading after jetting), Design for Imprint or DFI (to accelerate drop

spreading) and material engineering (to promote wetting between the resist and underlying adhesion layer). In addition, it is mandatory to maintain fast filling, even for edge field imprinting. Previously, we have demonstrated that it is feasible to fill dense line/space patterns in only one second.[17]

Figure 7 shows an experiment which demonstrates the impact of fill time on drop volume. By using smaller drop volumes, drops must be placed closer together, thereby minimizing the time it takes for drops to merge and fill the relief images on a mask. In the figure below, fill time is tracked over several years as drop volume is reduced from 35 picoliters to 1.0 picoliter. Fluid spread time is reduced almost two orders of magnitude. For further details on throughput, refer to the paper by Ye et al. in this Proceedings.

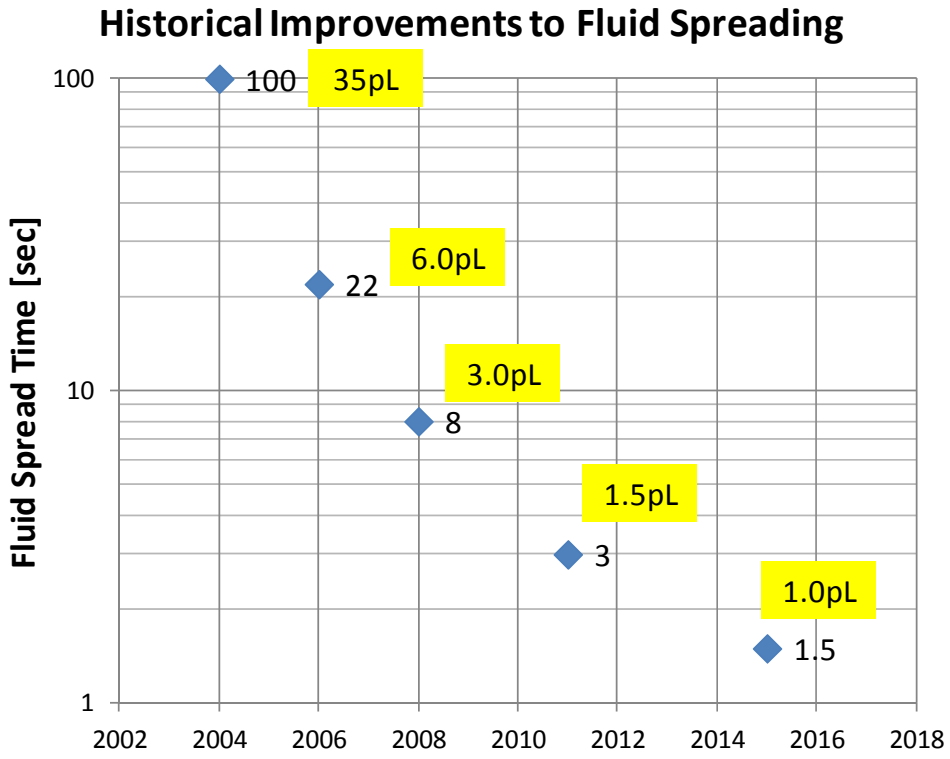


Figure 7. Fluid spread time as a function of resist drop volume. Spread time is reduced by almost two orders of magnitude by reducing the drop volume to 1 picoliter.

c. Defectivity and Particles

NIL like any lithographic approach requires that defect mechanisms be identified and eliminated in order to consistently yield a device. NIL does have defect mechanisms unique to the technology, and they include, liquid phase defects, solid phase defects and particle related defects.

Liquid phase defects can form as the result of contamination to the underlying adhesion layer. The result of this contamination is incomplete filling in a small area, and is typically referred to as a non-fill defect. This defect type has been addressed in the past by applying the same sort of environmental filtering systems required, for example, for chemically amplified resists.

Solid phase defects can occur during the separation process. Shear forces imparted between the mask and wafer can tear features and potentially leave resist on the imprint mask. Another consequence of shear forces is line collapse and can be observed when the aspect ratio of sub-20nm features starts to grow well beyond 2:1. These defect types have also been overcome by careful attention to system controls during separation and are also no longer considered a priority.

More troublesome are particles that reside and adhere to either the mask or wafer surface. In the past we have described how the inkjet system can add to particle count and how liquid in-line filtration systems addressed this issue.[18] These particle types were typically soft in nature and could be addressed by mask cleaning. Hard particles generated

within the imprint tool are the biggest source of concern. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process.

There are several countermeasures for particles that can be taken. Included on the list are:

- The minimization of particle generation from particle sources related to materials within the tool and the surface treatment of these materials
- The reduction of particles that could potentially find their way onto the mask and wafer. These can be addressed by optimizing the airflow within the tool and by providing an ionizer source to address charge build up on the mask
- The elimination of particles through an inspection and mask cleaning process flow.

Recent work has focused on material surface treatment and airflow control within the imprint tool. Test stand results indicate that a particle adder specification of 0.001 per wafer pass can be met, thereby sustaining a mask life of greater than 1000 wafers can be achieved. An example of the airflow within an imprint tool is shown in the simulation in Figure 8. For more details on mask life, readers are referred to the paper by Emoto et al. in this Proceedings.

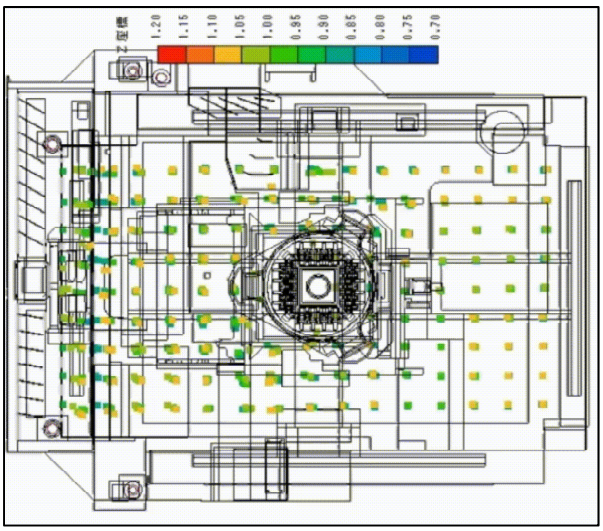


Figure 8. Air flow simulation in the imprint tool. Particles at the wafer plane have been minimized.

3. Imprint Systems

In 2015, the NZ2 was introduced. With a throughput an overlay specification of 10 wafers per hour and 8nm 3σ, respectively, the system was suitable for both integration work and pilot operation. To address high volume manufacturing, a cluster approach is required to meet throughput and cost of ownership requirements (CoO).

A schematic layout of a system containing four imprint stations is shown in Figure 9a. Four stations running at 60 wafers per hour provides a path for high volume manufacturing. The overlay specification is 6nm, 3σ. Integration of the NZ2C platform started in 2015 and an image of the tool is shown in Figure 9b. Development work will continue throughout 2016, with an introduction later in 2016.

Application of the system for sub-20nm NAND Flash devices has been discussed in the past. It is important to note, however, that dense contact patterns for DRAM and logic applications with a single mask are possible. Addressing both the DRAM and logic markets will require both improved overlay (in the case of DRAM) and improved defectivity (for logic devices).

Figure 9. a) Schematic image of the NZ2C cluster tool. b) Integration of the NZ2C system.

Conclusions

Great progress has been made in the field of nanoimprint lithography over the last two years. Overlay of better than 5nm (mean + 3sigma) has been demonstrated, and throughputs are starting to approach the numbers required for high volume manufacturing. Defectivity has been reduced by more than two orders of magnitude and several imprint specific defect mechanisms have been identified and eliminated. The continued reduction of particle adders extends both the life of the master mask and the replica mask. In this work, methods for improving overlay were explained. Wafer chucks with improved flatness reduce distortion at the wafer edge. To address higher order corrections, a two part solution was discussed. An array of piezo actuators can be applied to enable linear corrections. Additional reductions in distortion can then be addressed by the local heating of a wafer field.

The NZ2C cluster platform for high volume manufacturing was also presented. System development continues this year with a target for introduction later in 2016. The first application is likely to be NAND Flash memory, and eventual use for DRAM and logic devices as both overlay and defectivity improve.

Acknowledgments

The authors would like to thank their colleagues in the support of this work.

References

1. C. Bencher, Y. Chen, H. Dai, W. Montgomery, L. Huli, Proc. of SPIE Vol. 6924 69244E-1
2. Ping Xu, Yongmei Chen, Yijian Chen, Liyan Miao, Shiyu Sun, Sung-Woo Kim, Ami Berger, Daxin Mao, Chris Bencher, Raymond Hung, Chris Ngai, Proc. of SPIE Vol. 7973 79731Q-1.
3. S. Y. Chou, P. R. Kraus, P. J. Renstrom, "Nanoimprint Lithography", J. Vac. Sci. Technol. B 1996, 14(6), 4129 - 4133.
4. T. K. Widden, D. K. Ferry, M. N. Kozicki, E. Kim, A. Kumar, J. Wilbur, G. M. Whitesides, Nanotechnology, 1996, 7, 447 - 451.
5. M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, M. Wedlake, T. Michaelson, S. V. Sreenivasan, J. Ekerdt, and C. G. Willson, Proc. SPIE, Emerging Lithographic Technologies III, 379 (1999).
6. M. Colburn, T. Bailey, B. J. Choi, J. G. Ekerdt, S. V. Sreenivasan, Solid State Technology, 67, June 2001.
7. T. C. Bailey, D. J. Resnick, D. Mancini, K. J. Nordquist, W. J. Dauksher, E. Ainley, A. Talin, K. Gehoski, J. H. Baker, B. J. Choi, S. Johnson, M. Colburn, S. V. Sreenivasan, J. G. Ekerdt, and C. G. Willson, Microelectronic Engineering 61-62 (2002) 461-467.
8. S.V. Sreenivasan, P. Schumaker, B. Mokaberi-Nezhad, J. Choi, J. Perez, V. Truskett, F. Xu, X, Lu, presented at the SPIE Advanced Lithography Symposium, Conference 7271, 2009.

9. K. Selenidis, J. Maltabes, I. McMackin, J. Perez, W. Martin, D. J. Resnick, S.V. Sreenivasan, Proc. SPIE Vol. 6730, 67300F-1, 2007.
10. I. McMackin, J. Choi, P. Schumaker, V. Nguyen, F. Xu, E. Thompson, D. Babbs, S. V. Sreenivasan, M. Watts, and N. Schumaker, Proc. SPIE **5374**, 222 (2004).
11. T. Higashiki, T. Nakasugi, I. Yoneda, Proc. SPIE 7970 (2011).
12. Z. Ye, K. Luo, J. W. Irving, X. Lu, W. Zhang, B. Fletcher, W. Liu, M. Shafran, S. Lee, W. Longsine, V. Truskett, F. Xu, D. LaBrake, Douglas Resnick, S. V. Sreenivasan, Proc. SPIE. 8680, Alternative Lithographic Technologies V, 86800C. (March 26, 2013).
13. H. Takeishi and S. V. Sreenivasan, *Proc. SPIE*. 9423, Alternative Lithographic Technologies VII, 94230C. (March 19, 2015).
14. K. S. Selinidis, C. B. Brooks, G. F. Doyle, L. Brown, C. Jones, J. Imhof, D. L. LaBrake, D. J. Resnick, S. V. Sreenivasan, Proc. SPIE 7970 (2011).
15. Naoya Hayashi, "NIL Template: Progress and Challenges", Presented at the 2013 SPIE Advanced Lithography Symposium, 8680, February 25, 2013.
16. Koji Ichimura et al., *Proc. SPIE* 9423, Alternative Lithographic Technologies VII, 94230D (March 19, 2015).
17. N. Khusnatdinov, Z. Ye; K. Luo, T. Stachowiak, X. Lu, J. W. Irving, M. Shafran, W. Longsine, M. Traub, V. Truskett, B. Fletcher, W. Liu, F. Xu; D. LaBrake, S. V. Sreenivasan, Proc. SPIE. 9049, Alternative Lithographic Technologies VI, 904910. (April 08, 2014).
18. Z. Ye, K. Luo, J. W. Irving, X. Lu, W. Zhang, B. Fletcher, W. Liu, M. Shafran, S. Lee, W. Longsine, V. Truskett, F. Xu, D. LaBrake, D. Resnick, S. V. Sreenivasan, Proc. SPIE. 8680, Alternative Lithographic Technologies V, 86800C. (March 26, 2013).